

# Analyzing the Improvement in Efficiency through the Integration of Class-F Power Amplifiers Compared to Class-AB in an Envelope Tracking Architecture

Z. A. Mokhti, P. J. Tasker, J. Lees  
 Centre of High Frequency Engineering  
 Cardiff University  
 Wales, United Kingdom  
[amokhtiz@cardiff.ac.uk](mailto:amokhtiz@cardiff.ac.uk)

**Abstract**—This paper investigates the performance of a class-F mode power amplifier (PA) integrated in an envelope tracking (ET) environment, compared to the conventional class-AB mode of operation in the same setting. A 10W high voltage laterally diffused metal oxide semiconductor (HVLDMOS) device is used to perform the comparison at 900MHz using an active load pull system in an emulated ET environment at 900MHz. The analysis looks at three scenario of optimization: when the class-F and class-AB PA's are optimized at individual drain voltage within the ET range, optimized at peak drain voltage, and optimized at the average drain voltage. The challenges of maintaining the device in class-AB and class-F modes throughout the ET range due to the variation of the device output capacitance are also presented in terms of the trajectory of the fundamental and harmonic loads, as well as the degradation in drain efficiency.

**Keywords**—envelope tracking; high efficiency; class-F; class-AB.

## I. INTRODUCTION

Envelope tracking power amplifiers are becoming a more attractive solution to be deployed in 4G telecommunication infrastructure especially with the rise of small-cells. The implementation of Doherty power amplifiers to address the efficiency drop at output back-off condition is limited by its operating bandwidth due to the design of the quarter wavelength transformers that are used to combine the output of the main amplifier with the peaking amplifier. An envelope tracking architecture is therefore a more suitable choice to address the challenges of increasing signal bandwidth. Furthermore with the power consumption of PA's deployed in small cells are now comparable with other segments such as the digital pre-distortion (DPD), an ET architecture presents a more attractive solutions from a linearity point of view compared to the Doherty PA which requires a significant amount of pre-distortion [1].

Conventional envelope tracking architecture uses a class-AB mode of operation which provides a balance between efficiency and linearity. There have been examples of high-efficiency modes being implemented in an ET setting such as in [2] where an inverse class-F PA was used. However one of the main challenges in implementing high efficiency modes in

an ET setting is the variation of the device drain-to-source capacitance ( $C_{ds}$ ) with respect to drain voltage. Since ET uses a drain voltage modulation technique to improve efficiency at output back-off conditions, the  $C_{ds}$  value will also vary and this causes the optimum fundamental and harmonic loads at the package plane of the device to shift in a trajectory throughout the ET operating range.

This paper discusses the behavior of class-AB and class-F power amplifiers in an ET setting, the effect of  $C_{ds}$  to their overall efficiency, and the trajectory of their fundamental and harmonic load impedances as the drain voltage is varied in the ET environment.

## II. CLASS AB AND CLASS-F MODES

A class-AB power amplifier is biased somewhere between pinch-off (class-B) and mid-point of drain current range (class-A). The theoretical efficiency therefore ranges between these two classes, i.e. 50% to 78.5%. A class-AB PA is realized by terminating the 2<sup>nd</sup> harmonic load to a short circuit while the fundamental load is chosen to balance output power and efficiency. Examples of class-AB implementations include [3] where a 25W Gallium Nitride (GaN) device was used achieving a drain efficiency of 60% at 1.98GHz, and [4] where an 8W Gallium Arsenide (GaAs) device implemented in an ET setting achieved between 45% to 55% of power added efficiency.

A class-F power amplifier is able to achieve a high-efficiency mode by reducing the overlap between the half-rectified sine wave drain current and the squared drain voltage waveforms. The second and third harmonic loads are terminated in a short and an open circuit, respectively while the fundamental load is chosen to find a balance between efficiency and output power. The half-rectified current also has a lower DC component while the squared voltage waveform consists of a higher fundamental component. This combination improves the overall drain efficiency, as described in [5] and [6] where a drain efficiency of 78% is achieved for a 5W LDMOS device and 74% for a 10W Gallium Nitride (GaN) device, respectively.

While the high efficiency of class-AB and class-F PA's can be achieved at a particular drain voltage setting, it will inevitably degrade at other drain voltage settings due to the variation of the drain-to-source capacitance of the device.

### III. MEASUREMENT METHODOLOGY & SETUP

A waveform engineering approach is used to analyze the behavior of class-AB and class-F power amplifiers in an ET setting. The measurements are performed using an active load pull system capable of controlling up to the third harmonic load, as shown in Fig. 1. A non-linear vector network analyzer (NVNA) is used as the receiver and an external signal generator and a power amplifier are used to provide a continuous wave (CW) input signal at 900MHz. On the load side three signal generator-power amplifier pairs are connected to the output of the device under test (DUT) to emulate the reflected waves, with circulators used to isolate these signals from the output signal from the DUT. A rigorous de-embedding process is applied to shift the reference plane to the device current generator plane, taking into account the variation in  $C_{ds}$  for different drain voltage settings.

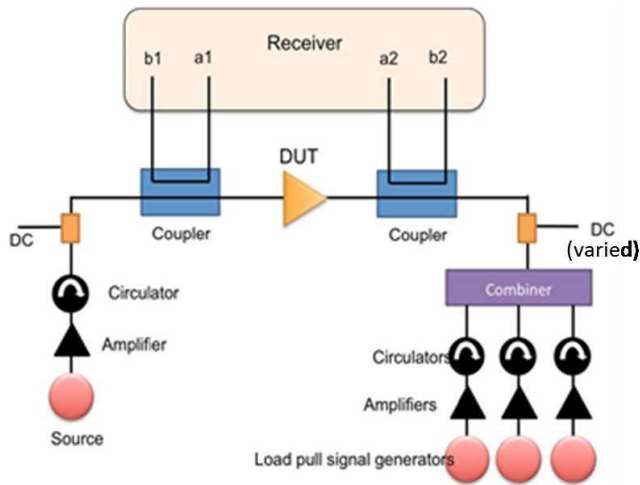


Fig. 1. Active load pull system used to emulate the loads in an ET setting

A 50V high voltage laterally diffused metal oxide semiconductor (HVLDMOS) device is emulated in these modes using the active load pull system. The allowable operating drain voltage range in this experiment is set between 16V and 48V to avoid the knee and the breakdown regions, respectively. To emulate an ET setting, the drain voltage is stepped from 16V to 48V in 4V steps.

The device is biased in a class-AB mode at 3% of maximum drain current and driven 3dB into compression. The fundamental load is optimized for efficiency while the second harmonic load is initially terminated with a short circuit and then optimized using a harmonic load pull search. The drain voltage is stepped within the ET range to emulate the ET environment.

The same device is then biased to a class-F mode of operation where the 2<sup>nd</sup> and 3<sup>rd</sup> harmonic loads are terminated in a short circuit and an open circuit, respectively. For this mode the device is driven 1dB into compression where the

fundamental is optimized for efficiency just as in the case of the class-AB PA. The ET emulation step is repeated.

There are three scenario that are investigated in this comparison analysis: (a) an ideal case where the class-AB and class-F conditions are maintained throughout the ET range, (b) when the class-AB and class-F loads are optimized at 48V which is the peak of the ET range, and (c) where the loads are optimized at the average drain voltage of 28V. The 28V drain voltage is selected as it represents the voltage where the PA will spend most of its time when it is excited with an LTE modulated signal the peak drain, as calculated from [1].

### IV. RESULTS & DISCUSSIONS

#### A. Class-AB and Class-F in ET Optimized at Individual Drain Voltages (Ideal Case Scenario)

This scenario gives an indication of the best possible drain efficiency that these modes can achieve in the ET range, if the effect of  $C_{ds}$  is removed. In this setup, the device is de-embedded using a dynamic  $C_{ds}$  value that corresponds to the drain voltage being set. The fundamental loads for both class-AB and class-F are optimized for efficiency as this is the parameter of interest for this work. In the case of class-AB the 2<sup>nd</sup> harmonic load is found to be optimum at a 40-degree shift in phase from an ideal short circuit, while for class-F the 2<sup>nd</sup> harmonic is found to be optimum at the short circuit and at the open circuit for the 3<sup>rd</sup> harmonic load. These harmonic terminations are used for each drain voltage setting throughout the ET emulation steps, keeping in mind the difference  $C_{ds}$  de-embedding requirements at the same time. Therefore at the package plane of the device, the resulting loads shift in a trajectory on the Smith chart as the drain voltage is changed from 16V to 48V in 4V steps, as shown in Fig. 2.

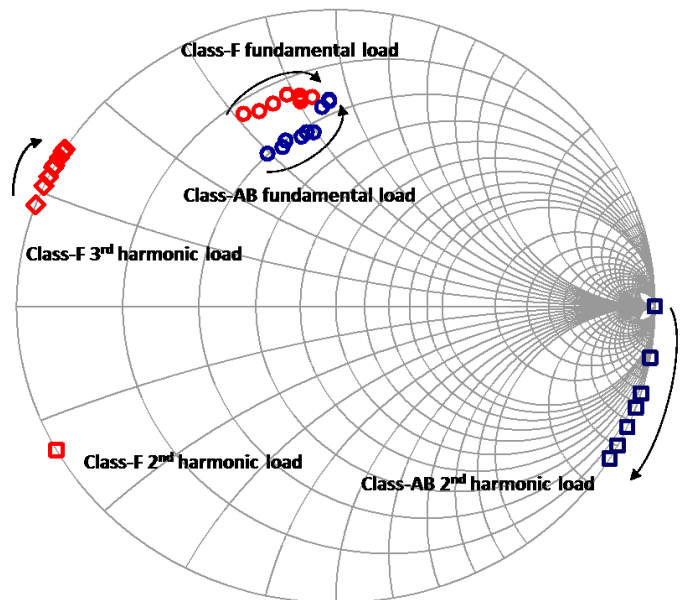


Fig. 2. The trajectory of the fundamental and harmonic loads at the package plane of the DUT. The direction of the arrows indicate the direction of increasing drain voltage from 16V to 48V.

For class-AB, the second harmonic load impedance shifts following a trajectory shown in Fig. 2 since at the current generator plane it is terminated at an angle of  $-140^\circ$  along the perimeter of the Smith chart instead of a perfect short circuit as was the case for class-F.

The resulting locus of each setting's drain efficiency is shown in Fig. 3. As expected, the class-F has a higher drain efficiency which peaked at 74% compared to the class-AB mode which has a peak efficiency of 65%.

### B. Class-AB and Class-F Optimized at Peak Drain Voltage of 48V

In this scenario, the fundamental and harmonic loads of the class-AB and class-F PA's are set when the device is operating at 48V drain bias, taking into consideration the corresponding  $C_{ds}$  value at this peak drain voltage. Using this fixed load combination, the drain voltage is then stepped from 48V to 16V in 4V steps, and for each step a suitable drive level is set to maintain about 3dB compression point for class-AB and 1dB for class-F.

As observed in Fig. 3, the drain efficiency of the class-AB dropped from about 64% at peak power to 50% at 9dB output back-off. The efficiency of the class-F PA also dropped from 73% to 57% in that same output back-off range. Fig. 4 shows the time-domain waveforms of the drain current and voltage of these 2 PA modes as the drive level and drain bias voltage is stepped down. For the class-AB PA, the drop in efficiency is caused by the non-optimum fundamental load as the drain is varied to 16V. Another observation is that there is an increase in the overlapping region between the current and the voltage at the lower drain voltage settings. For the class-F current waveform, bifurcations start to occur at the lower drain voltage settings that correspond to the lower output power level. This is caused by the phase shift in the harmonic content due to non-optimum impedance termination resulting in the drop in efficiency.

### C. Class-AB and Class-F Optimized at Average Operating Drain Voltage of 28V

This setting is similar to the previous scenario except that the loads are set when the device is operating at 28V, which is the drain voltage that the PA will spend most of its time when excited with an LTE signal. The drain efficiency now is peaked somewhere in the middle of the PA output power range instead of at peak power. For the class-AB PA, the lowest efficiency is 57% which occurs at the lowest output power range, which is 5%-point drop from the ideal case, instead of a 9%-point drop as in the previous scenario. Another observation is that this load environment enables a higher output power at the higher drain voltage setting, with a maximum output power of 39.6dBm delivered to the load. For the class-F the average efficiency also improved, with the efficiency throughout the ET range maintained above 64%. Bifurcations still occur in the class-F current waveforms on both ends of the ET range as shown in Fig. 5, but are less severe compared to when the device is optimized at 48V.

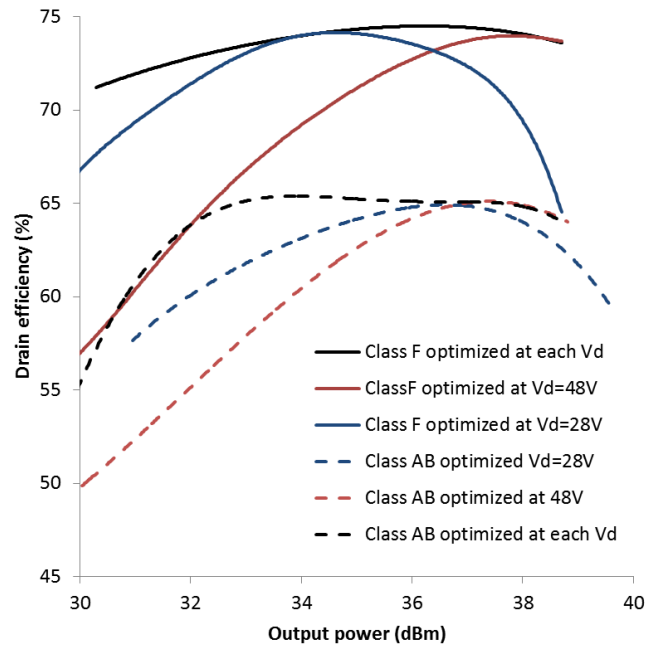


Fig. 3. The overall drain efficiency for class-AB and class-F for the 3 scenario discussed

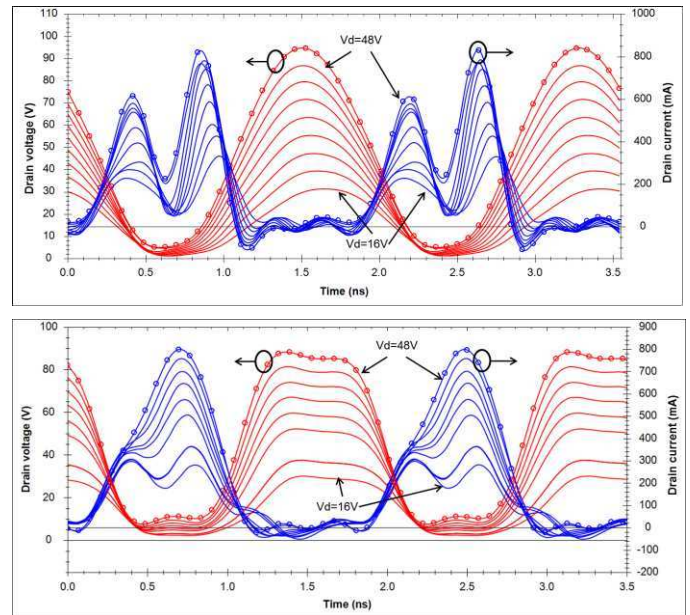


Fig. 4. The time-domain current and voltage waveforms of the class-AB PA (above) and the class-F PA (below), when the PA's are optimized at 48V bias.

## V. CONCLUSIONS

A comparison of class-AB and class-F modes in an ET setting has been presented. A waveform engineering approach is used to emulate these modes on the same HVLD MOS device at 900MHz. The trajectory of the fundamental and harmonic load impedances to maintain the device in class-AB and class-F modes throughout the ET range is also shown. For this device, if the operating drain voltage range is between 16V and 48V, optimizing the class-F when the device is biased at 28V

drain voltage achieves the best overall efficiency when used in an LTE signal amplification.

[6] V. Carrubba, J. Lees, J. Benedikt, P.J. Tasker, and S.C. Cripps, "A novel highly efficient broadband continuous class-F RFPA delivering 74% average efficiency for an octave bandwidth," Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International.

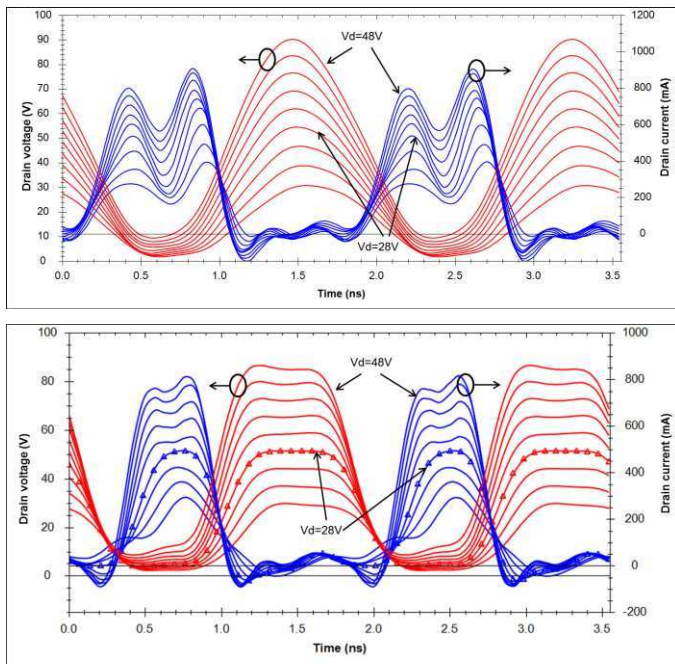


Fig. 5. The time-domain current and voltage waveforms of the class-AB PA (above) and the class-F PA (below), when the PA's are optimized at 28V bias.

ACKNOWLEDGMENT

This research is supported by the OPERA-Net 2 project working to reduce the overall environmental impact of mobile radio networks. The authors also would like to thank Freescale Semiconductor for providing additional support for this research.

REFERENCES

[1] M. Lassanen et al, "Environmental friendly radio networks: Approaches of the European OPERA-Net 2 project", 2013 20<sup>th</sup> International Conference on Telecommunications

[2] J.H. Kim et al, "High-efficiency envelope tracking transmitter with optimized class-F<sup>-1</sup> amplifier and 2-bit envelope amplifier for 3G LTE base station," IEEE Transaction on Microwave Theory and Techniques, Vol. 59, No. 6, June 2011.

[3] Z. Yusoff, J. Lees, J. Benedikt, P.J. Tasker, S.C. Cripps, "Linearity improvement in RF power amplifier system using integrated Auxiliary Envelope Tracking system," Microwave Symposium Digest, 2011 IEEE MTT-S International.

[4] A. Brackle, M. Ott, S. Heck, M. Berroth, "An 8W GaAs Class-AB amplifier for operation in envelope tracking systems", 2011 German Microwave Conference (GeMIC).

[5] A. Sheikh et al, "Systematic waveform engineering enabling high efficiency modes of operation in Si LDMOS at both L-band and S-band frequencies", Microwave Symposium Digest, 2008 IEEE MTT-S International.